In the Claims:

1 **Please amend Claim 1 as follows.**

2

3   1.   (Twice Amended) A data processing system
4 comprising:

5   a master-state data processing unit;

6   a communication bus, the master-state data
7 processing unit exchanging asynchronous transfer mode
8 protocol signals with the bus; and

9   at least one slave-state data processing unit, the
10 slave-state data processing unit including:

11   a central processing unit;

12   a direct memory access unit coupled to the
13 central processing unit, and

14   a Utopia mode interface unit coupled to the
15 direct memory access unit, <u>the Utopia interface unit</u>
16 <u>acting in a receive mode and in a transmit mode</u>; the
17 Utopia transfer mode interface unit having:

18   a processor coupled to the communication
19 bus and exchanging asynchronous transfer mode protocol
20 signals therewith; and

21   a buffer memory unit, the buffer memory
22 unit buffering data signals between the direct memory
23 access unit and the processor, wherein the transfer of
24 data cells between the buffer memory unit and the direct

1 memory interface unit is determined by an event signal,

2 the event signal indicating to the direct memory access

3 unit that a data cell is stored in the buffer memory unit

4 in the receive mode, the event signal indicating to the

5 direct memory access unit that space for a data cell is

6 available in buffer memory unit in the transmit mode.

7

8   2.   (Cancelled)   ~~The data processing system as~~

9 ~~recited in claim 1 wherein the Utopia interface unit can~~

10 ~~act in a receive mode and in a transmit mode.~~

11

12   3.   (Original)   The data processing system as

13 recited in claim 1 wherein the buffer memory unit is a

14 first-in/first-out memory unit.

15

16   4.   (Original)   The data processing system as

17 recited in claim 1 wherein the processor includes:

18   an input interface unit; and

19   an output interface unit; and wherein the buffer

20 memory unit includes:

21   an input buffer memory unit, wherein the transfer

22 between the input buffer memory unit and the direct

23 memory access unit is determined by a receive event

24 signal; and

25   an output buffer memory unit, wherein the transfer

26 between the direct memory access unit and the output

27 buffer memory unit is determined by a transmit event

28 signal.

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PAGE 4/15 * RCVD AT 5/26/2005 2:30:49 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/0 * DNIS:7464000 * CSID: * DURATION (mm-ss):04-28

1   5.   (Original)   The data processing system as
2   recited in claim 4 wherein data is transferred from the
3   communication bus to the input buffer memory unit, and
4   wherein data is transferred from the output buffer memory
5   unit to the communication unit through the output
6   interface unit.

7

8   6.   (Original)   The data processing system as
9   recited in claim 5 wherein in the input buffer memory
10   unit and the output buffer memory units are first-
11   in/first-out memory units.

12

13   7.   (Original)   The data processing system as
14   recited in claim 4 wherein the receive event signal is
15   generated when the buffer memory unit has a complete data
16   cell stored therein, the receive event signal being
17   cleared when transfer between the buffer memory unit and
18   the direct memory access unit is begun, and wherein the
19   transmit event signal is generated when the buffer memory
20   unit has space for a complete data cell, the transmit
21   event signal being cleared when the transfer of the data
22   cell to the buffer memory unit from the direct memory
23   access unit is begun.

24

25   **Please amend Claim 8 as follows.**

26

27   8.   (Twice amended)   A data processing system
28   comprising:

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1   at least one slave-state data processing unit;

2   a communication bus, the master-state data
3   processing unit exchanging asynchronous transfer mode
4   protocol signals with the bus; and

5   a master-state data processing unit, the master-
6   state data processing unit including:

7   a central processing unit;

8   a direct memory access unit coupled to the
9   central processing unit, and

10   a Utopia interface unit coupled to the direct
11 memory access unit; the Utopia interface unit having:

12   a processor coupled to the communication
13 bus and exchanging asynchronous transfer mode protocol
14 signals therewith; and

15   a buffer memory unit, the buffer memory
16 unit buffering data signals between the direct memory
17 access unit and the processor, an event signal indicating
18 to the direct memory access unit when a data cell has
19 been received by the buffer memory unit in a receive
20 mode, an event signal indicating to the direct memory
21 access unit that space for a data cell is available in
22 the receive mode.

23

24   9.   (Original)   The data processing system as
25 recited in claim 8 wherein the processor includes:

26   an input interface unit; and

1   an output interface unit: and wherein the buffer

2   memory unit includes;

3   an input buffer memory unit; and

4   an output buffer memory unit.

5

6   10. (Original)   The data processing system as
7   recited in claim 9 wherein the data is transferred from
8   the communication bus through the input interface unit to
9   the input buffer memory unit, and wherein data is
10 transferred from the output buffer memory unit through
11 the output interface unit to the communication bus.

12

13 11. (Original)   The data processing system as
14 recited in claim 10 wherein the input buffer memory unit
15 and the output buffer memory unit are first-in/first-out
16 memory units.

17

18 12. (Original)   An Utopia interface unit for
19 providing an interface between an external data
20 processing unit and a direct memory access unit, the
21 interface unit comprising:

22   an input buffer memory unit, the input buffer memory
23 unit providing data cells to the direct memory interface
24 unit, the input buffer unit applying an event signal to
25 direct memory access unit indicating that space is
26 available for a data cell in a transmit mode, the inp9ut
27 buffer applying an event signal to the direct memory

1 access unit indicating that data cell is stored therein

2 in a receive mode;

3   an interface input unit, the interface input unit

4 controlling the transmission of data cells from the

5 external processing system to the input buffer memory

6 unit;

7   an output buffer memory unit, the output buffer

8 memory unit receiving data cells from the direct memory

9 access unit; and

10   an interface output unit, the interface output unit

11 controlling transmission of data cells from the output

12 buffer memory unit to the external processing system.

13

14   13. (Original)   The interface unit as recited in

15 claim 12 wherein the input buffer memory unit and the

16 output buffer memory unit are first-in/first-out memory

17 units.

18

19   14. (Original)   The interface unit as recited in

20 claim 12 wherein the first-in/first-out memory units can

21 store at least two data cells.

22

23   15. (Original)   The interface unit as recited in

24 claim 12 wherein data from the input buffer memory unit

25 is transferred to the direct memory access unit in

26 response to word-read signal from the buffer memory unit.

27

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1   16.   (Original)   The interface unit as recited in
2   claim 12 wherein data from the direct memory unit is
3   stored in the output buffer memory unit in response to a
4   word-write signal from the output buffer memory unit.

5

6   17.   (Original)   The interface unit as recited in
7   claim 12 wherein data is transferred from the external
8   processing unit to the input buffer unit in response to
9   the cell-available signal from the input buffer unit.

10

11   18.   (Original)   The interface unit as recited in
12   claim 12 wherein data is transferred from the output
13   buffer memory unit to the external processing unit in
14   response to cell-available signal from the output buffer
15   memory unit.

16

17   19.   (Original)   The interface unit as recited in
18   claim 12 wherein the interface unit is operating in a
19   slave mode, the transfer of data cells from the input
20   buffer memory unit and the direct memory access unit
21   being determined by a receive event signal, the transfer
22   of data cells from the direct memory access unit to the
23   output buffer memory unit being determined by a transmit
24   event signal.

25

26   20.   (Original)   The data processing system as
27   recited in claim 19 wherein the receive event signal is
28   generated when the input buffer memory unit has a

1 complete data cell stored therein, the receive event

2 signal being cleared when transfer between the input

3 buffer memory unit and the direct memory access unit is

4 begun, and wherein the transmit event signal is generated

5 when the output buffer memory unit has space for a

6 complete data cell, the transmit event signal being

7 cleared when the transfer of the data cell to the output

8 buffer memory unit from the direct memory access unit is

9 begun.

10

11 **Please add claim 21.**

12

13   21.   (Newly Added) The data processing system as

14 recited in claim 12 wherein the receive event signal is

15 generated when the buffer memory unit has a complete data

16 cell stored therein, the receive event signal being

17 cleared when transfer between the buffer memory unit and

18 the direct memory access unit is begun, and wherein the

19 transmit event signal is generated when the buffer memory

20 unit has space for a complete data cell, the transmit

21 event signal being cleared when the transfer of the data

22 cell to the buffer memory unit from the direct memory

23 access unit is begun.